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Examining Group 2186

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS : Manoj Khare et al.
SERIAL NO. : 09/749,660
FILED : December 28, 2000
FOR : METHOD AND APPARATUS FOR REDUCING
MEMORY LATENCY IN A CACHE COHERENT
MULTI-NODE ARCHITECTURE
GROUP ART UNIT : 2186
EXAMINER : Tuan V. Thai
ASSIGNEE : INTEL CORPORATION

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AMENDMENT

S I R:

The following amendments and remarks below are respectfully submitted in
response to the Office Action dated June 3, 2004.